GaAs MESFET OSCILLATOR DESIGN USING LARGE-SIGNAL S-PARAMETERS

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ABSTRACT

A novel analytical technique is presented which uniquely determines the embedding network required for a MESFET oscillator to deliver specified power to an arbitrary load. An experimental 5.3 GHz oscillator provided 24 dBm with 35% efficiency.

Introduction

Current approaches to oscillator design using transistors typically involve the reduction of the two-port device to a one-port configuration by embedding it in a suitable circuit[1]. The topology is usually chosen to resonate the input port so that the stability factor is less than unity at the frequency of operation; an output circuit is then designed to match the resulting negative output impedance. While yielding practical oscillators, this approach gives no information about the maximum power that can be generated by the transistor, or the output impedance needed to obtain it.

This paper presents a systematic approach to oscillator design using large-signal S-parameters. It enables the analytical synthesis of an embedding circuit for the transistor, which will ensure oscillation into a given load at maximum power and at a specified frequency. The approach differs from previously reported two-port bipolar oscillator design techniques using Y-parameters[2,3], in that

(i) it is directly applicable at microwave frequencies and to GaAs MESFETs in particular, for which large-signal S-parameters can be measured, and,

(ii) it allows the easy incorporation of lengths of transmission line as matching elements, thereby ensuring physical realizability of the design.

Since this approach is based on the use of large-signal S-parameters, it is first necessary to establish their validity. S-parameters represent the response of a linear system by means of superposition of voltage waves. In order to apply them to describe a nonlinear element such as a transistor, its response to large-signal excitations present at both its input and output terminals must first be linearized about each operating point of interest. Certain restrictions must then be applied to ensure that this quasilinear response can be decomposed into a unique S-parameter representation. A sufficient set of imposed restrictions can be stated as follows[4]:

a) Only sinusoidal voltages are present. The effect of harmonic voltages and their terminations are neglected.

b) The input S-parameters S_{11} and S_{21} are functions of only the incident input power $|V_1^+|^2$, and the output S-parameters S_{12} and S_{22} are functions of only the power incident on the output port of the device, $|V_2^+|^2$.

Quasilinearization with Large Signal S-Parameters

Making these assumptions, the S-parameter quasilinear representation of device operation may be written:

$$V_1^- = S_{11}(|V_1^+|)V_1^+ + S_{12}(|V_2^+|)V_2^+ \qquad (1a)$$

$$V_2^- = S_{21}(|V_1^+|)V_1^+ + S_{22}(|V_2^+|)V_2^+ \quad , \qquad (1b)$$

where V_1^+ and V_2^+ represent the incident voltage waves, and V_1^- and V_2^- the reflected voltage waves, at the input and output ports, respectively.

In order to verify the above assumptions for a common-source FET, both computer simulations[4], using a nonlinear representation for the FET with its parasitic circuit elements[5], and physical measurements, to examine device behavior, have been made.

Consider Eq. (1a). When the device is simultaneously driven at both input and output ports by incident voltages V_1^+ and V_2^+, the reflection coefficient Γ_1, at the input is given by

$$\Gamma_1 = \frac{V_1^-}{V_1^+} = S_{11}(|V_1^+|) + S_{12}(|V_2^+|)\left|\frac{V_2^+}{V_1^+}\right| e^{j\phi} \qquad (2)$$

where ϕ is the phase difference between V_1^+ and V_2^+. If, now, $|V_1^+|$ and $|V_2^+|$ are held constant, and ϕ is varied, the locus of Γ_1 should be a circle with center $S_{11}(|V_1^+|)$ and radius $S_{12}(|V_2^+|)\left|\frac{V_2^+}{V_1^+}\right|$. Any deviation from a circular locus provides an indication of departure from the linearized behavior assumed in Eq. (1a).

The transistor selected for the simulations and experiments was a NEC-869177, which is a carrier mounted, single-cell chip for use up to Ku band. The gate length is 0.5 microns, and gate width 750 microns. For amplifier applications, this transistor has an output power of 22 dBm at 11 GHz at the 1dB gain compression point. Figure 1 shows the locus of Γ_1 for an

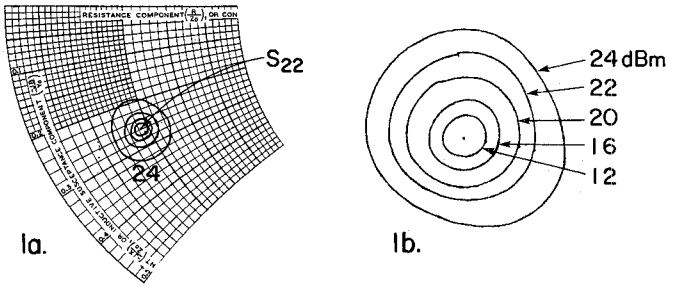

Fig. 1a. Locus of Γ_1 for $|V_1^+|^2$ = 20 dBm as a function of $|V_2^+|^2$ as the phase between V_1^+ and V_2^+ is varied.

1b. Expanded view of the loci for several $|V_2^+|^2$.

incident power on port 1 at 10 GHz (the gate) of 19.3 dBm, when the device is simultaneously driven with incident power on port 2 (the drain) of 12, 16, 20, 22, or 24 dBm. The transistor was heavily saturated during the 24dBm measurement, as the gate-drain junction was in reverse saturation giving rapidly increasing DC gate current. It was observed, in general, that non-circular loci were associated with high DC gate currents. Qualitatively, the curves indicate that the

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use of Eq. (1a) is reasonable up to $|V_2^+|$ corresponding to 22 dBm with an incident $|V_1^+|$ corresponding to 19.3 dBm. The locus of Γ_2 shows similar behavior[4].

Oscillator Network Synthesis

Figure 2 shows an oscillator comprising an FET embedded in an external circuit. The load is incorporated into the external circuit so that the effect of any mismatch and loading may be included in the design. The incident wave $|V_1^+|$ is fixed at the outset of the design; $|V_2^+|$ is initially estimated and then iterated until a self-consistent solution is found, as described below.

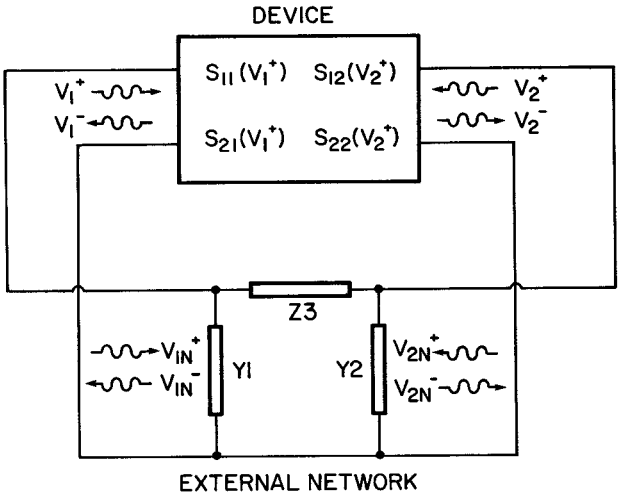

Fig. 2. Oscillator topology for a shunt embedding circuit. The device is represented by large-signal S-parameters. The incident and reflected voltage waves are shown.

The quantity V_2^- is a free parameter. By defining the complex voltage gain $A = V_2^-/V_1^+$, the power delivered to the external network can be maximized as a function of A. Equating the negative of the device impedance to the circuit input impedance at each port, and by representing the embedding network by its inverse S-parameters, $\$^{-1}$, the condition for oscillation is found to be

$$S_{22}\$_{11}^{-1} + \$_{12}^{-1}(A-S_{21}) - S_{11}S_{22} + S_{12}S_{21} - AS_{21} = 0$$
$$S_{22}\$_{21}^{-1} + \$_{22}^{-1}(A-S_{21}) - AS_{22} = 0 \qquad (3)$$

A set of four design equations is obtained by equating real and imaginary parts in each of these equations to zero.

In Eq. (3), the S_{ij} are the large-signal device S-parameters. The unknowns are the network elements responsible for $\$_{ij}^{-1}$ and the lengths and impedances of transmission lines connecting the device to the network. Only four unknowns can be determined from Eqs. (3). The rest are free parameters to be specified by other constraints such as lossless feedback elements, physical realizability, etc.

Optimization of $A = V_2^-/V_1^+$, keeping V_1^+ constant, requires that V_2^- be varied in both magnitude and phase until the power delivered to the external network is a maximum. Referring to Fig. 2, if the only lossy element in the external network is the load, the power delivered is given by

$$P = |V_1^-|^2 - |V_1^+|^2 + |V_2^-|^2 - |V_2^+|^2 \quad .$$

By expressing the voltage waves in terms of the FET S-parameters and A, and differentiating, the value of A for maximum power can be found as

$$A_{opt} = \frac{1}{|S_{22}|^2+|S_{12}|^2-1}\left(|S_{12}|^2S_{21}-S_{21}-S_{22}S_{11}S_{12}^*\right) \qquad (4)$$

This optimum gain, A_{opt}, varies with V_1^+ and V_2^+ because the S_{ij} depend on them. In the design, V_1^+ is chosen and an iterated value of V_2^+ can be calculated directly by using the S_{ij} found with the initial values of V_1^+ and V_2^+, and substituting $V_2^- = A_{opt}V_1^+$ into Eq. (1b) to obtain

$$V_2^+ = \left[\frac{A_{opt} - S_{21}(|V_1^+|)}{S_{22}(|V_2^+|)}\right] V_1^+ \qquad (5)$$

If a self-consistent result is not obtained from Eq. (5) V_2^+ is adjusted, new S_{ij} and A_{opt} found and the process is repeated. Once the correct V_2^+ is found for a given V_1^+, the maximum power that can be obtained from the transistor may be calculated. By then varying $|V_1^+|$, the maximum power is found to peak (at the point of maximum power-added efficiency) at a particular value of $|V_1^+|$, which is chosen as the design point. The unknown circuit elements are then found by solution of Eqs. (3).

Oscillator Design

An oscillator was built using the circuit predicted by this design approach. A π-topology was chosen for the feedback network, with the device reference planes extended by transmission line lengths that were incorporated into this network.

Table I. Design Values for 5 GHz Oscillator

Case		$\lvert V_1^+\rvert^2$ (dBm)	$\lvert V_2^+\rvert^2$ (dBm) Est.	Calc.	A_{OPT}	$P_{LOAD}/\lvert V_1^+\rvert^2$	P_{LOAD} CALC. (mW)
1	x	17.7	19.9	24.6	2.77+j1.56	5.16	-
	✓	17.7	21.2	20.9	2.07+j1.37	4.00	235
2	x	19.3	19.9	26.0	2.67+j1.54	4.86	-
	✓	19.3	22.0	21.1	1.82+j1.35	3.52	300
3	x	20.7	26.4	16.4	.678+j1.45	2.05	-
	x	20.7	19.9	26.1	2.30+j1.36	3.55	-
	x	20.7	23.4	19.1	1.27+j1.24	2.28	-
	✓	20.7	22.0	21.3	1.51+j1.25	2.55	300
4	x	22.0	23.4	19.3	.998+j1.17	1.61	-
	✓	22.0	22.0	21.4	1.25+j1.15	1.82	288

Table 1 illustrates the steps in the design of a 5 GHz oscillator to operate into a 50Ω load. The first column groups blocks of data according to the value of $|V_1^+|^2$ (incident input power) selected. The final line in each block, indicated by a ✓, is that for which the estimated value of $|V_2^+|^2$ (incident power at the output) agrees with the correct solution given by Eq. (5). For example, in the first line of block 1, an incident input power of 17.7 dBm was chosen, and an incident power of 19.9 dBm estimated. With these values, the large-signal S-parameters are defined, and A_{opt} is found from Eq. (4)

to be 2.77+j1.56; using this in Eq. (5) gives $|V_2^+|^2$, corresponding to 24.6 dBm. Thus, the estimate of incident power at port 2 must be increased, as in the second line of block 1. This changes $S_{12}(|V_2^+|)$ and $S_{22}(|V_2^+|)$, and after recalculation, the new incident output power is found to be close to that initially assumed.

Cases 2, 3, and 4 show the results obtained by selecting higher values of incident input power. The predicted output power does not continue to increase with $|V_1^+|^2$, but reaches a peak of 300 mW in case 2 and 3. This is then the desired operating point. Case 2 was used rather than case 3 because of the better accuracy in the application of S-parameters at the lower input power level, since the FET is not saturated as much. The peaking of the maximum output power with $|V_1^+|^2$ represents the behavior of the power-added efficiency curve for the FET.

The values of the S-parameters at the desired operating point are then used with the value of A_{opt} in a root finding routine to solve Eqs. (3) for the network elements. The resulting circuit is shown in Figure 3.

The experimental oscillator operated at 5.3 GHz and generated 250 mW of power with a DC to RF conversion efficiency of 32%. The second harmonic was down 18 dB at this point. By increasing the drain voltage to 9V, a peak output power of 25 dBm (300 mW) was

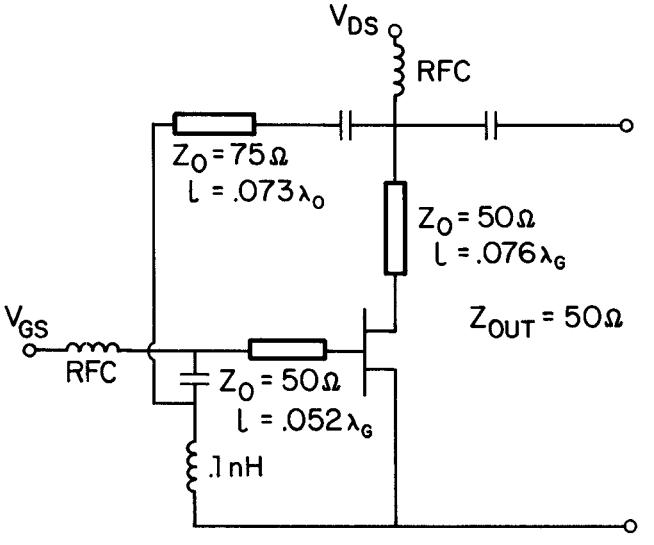

Fig. 3. Predicted oscillator circuit for the shunt topology chosen. The blocking capacitors used were 100 pF.

obtained. Figure 4 presents plots of output power and efficiency. The oscillator was also operated in a self-biased mode from a single drain supply, and yielded an efficiency of 35%.

In conclusion, an analytical method is presented which permits the design of feedback oscillators which deliver maximum power into an arbitrary load. This method may prove valuable in the design of high efficiency circuits and for monolithic FET oscillators and amplifiers.

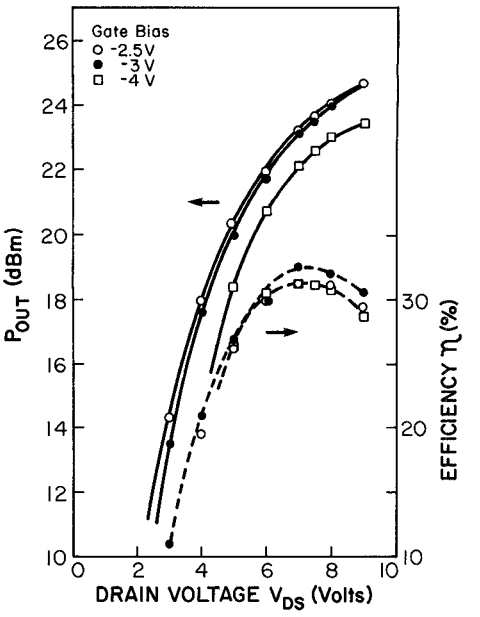

Fig. 4. Oscillator efficiency and power output as a function of drain voltage with gate voltage as the parameter.

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